

REVISION HISTORY

Version	Date	Engineer	Change Description
R0A	2020/2/12	Jamei Chu	Initial release
	2020/3/26	Jamei Chu	P.18 add 0.1uF cap. on MAC Rx side from PHY. P.25 remove U10 EEPROM (0x57) P.32 change OSC1 from 25MHz to 50MHz for FPGA. add AC couple cap. 0.1uF @ GBIT_125M_P/N (from 30773 to FPGA) P.50 change all DC-DC BST cap. package from 0402 to 0603. P.56 change L112 from 28A to 10A rating. (VCC1V0@3.5A) change VCC1V0 cap. C1140 from 560uF *2 to 100uF*2 P.31 add 0ohm res. @ DDR_TEN to FPGA P.15 modify DDR power VDDQ (BCM88272_DDR_VDDO) connect to MAC DDR VDDQ power. add R49 1K pull low @ DDR_RESET_N. add decoupling cap. at VCC0V6 to GND. add decoupling cap. at VDD1P2_DDR_VDD to VCC0V6. P.19 remove C233 470uF cap. @ BCM88272_PCIE_PVDD1P0 P.17 remove C188 @ BCM88272_RESCAL P.41 change C931 C932 to 0ohm res. @ BCM54140_SYNC_IN & SYNC/IO P.43 connect RJ3 LED power to VCC3V3
	2020/4/17	Jamei Chu	change partial MLCC from X5R to X7R for better temperature performance P.49 change CLK gen to 8P49N344-102NBGI8 for better jitter.
	2020/4/21	Jamei Chu	P.38 remove LB44 CB293 near USB conn. as cap. between gnd & chassis gnd is enough. P.31 change BCM54140_125M_SYNC from FPGA pin. M21 to pin. A22

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Custom	P002_Index List	Jamel					
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High Level Diagram

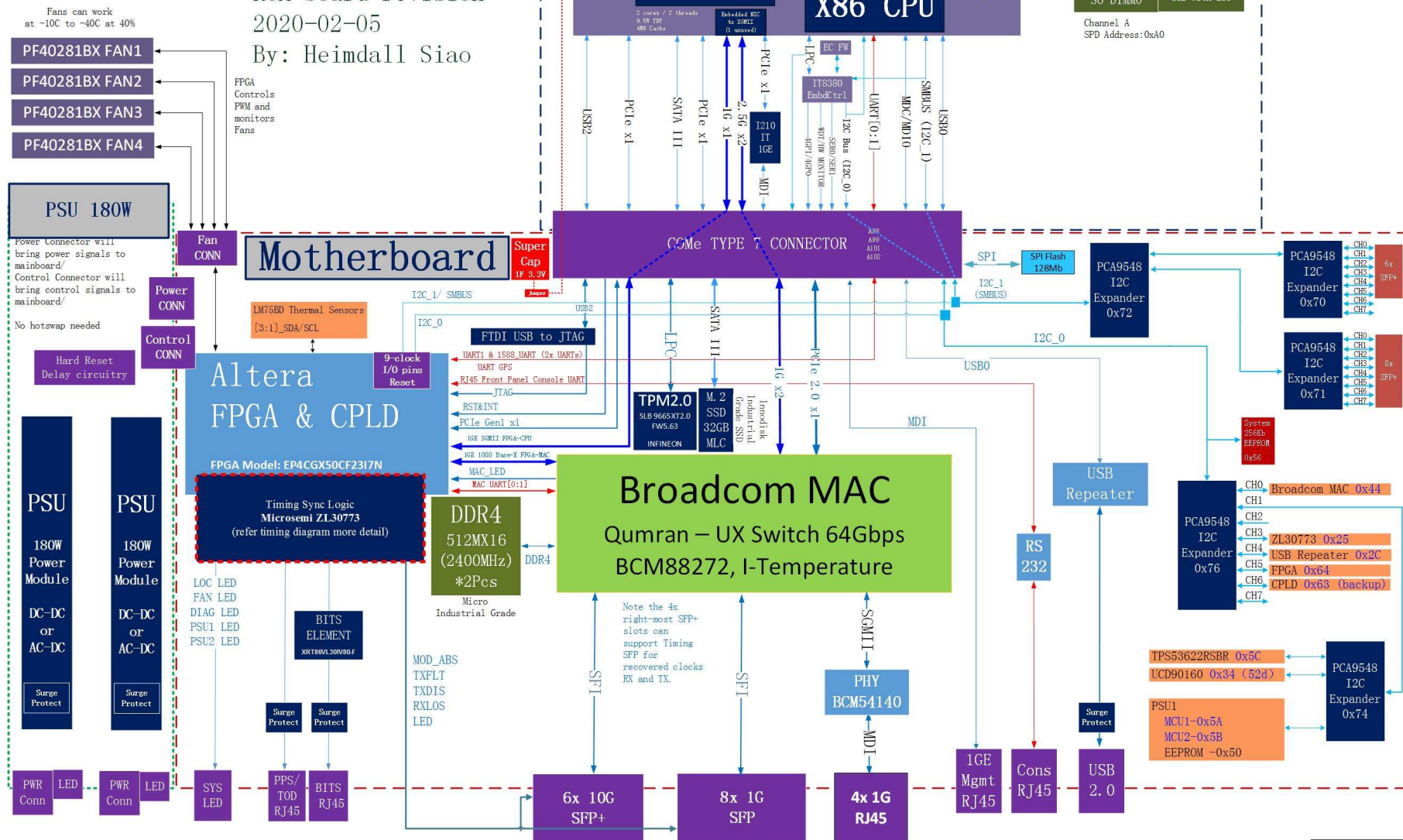
Accton Group

AS5915-18X Project

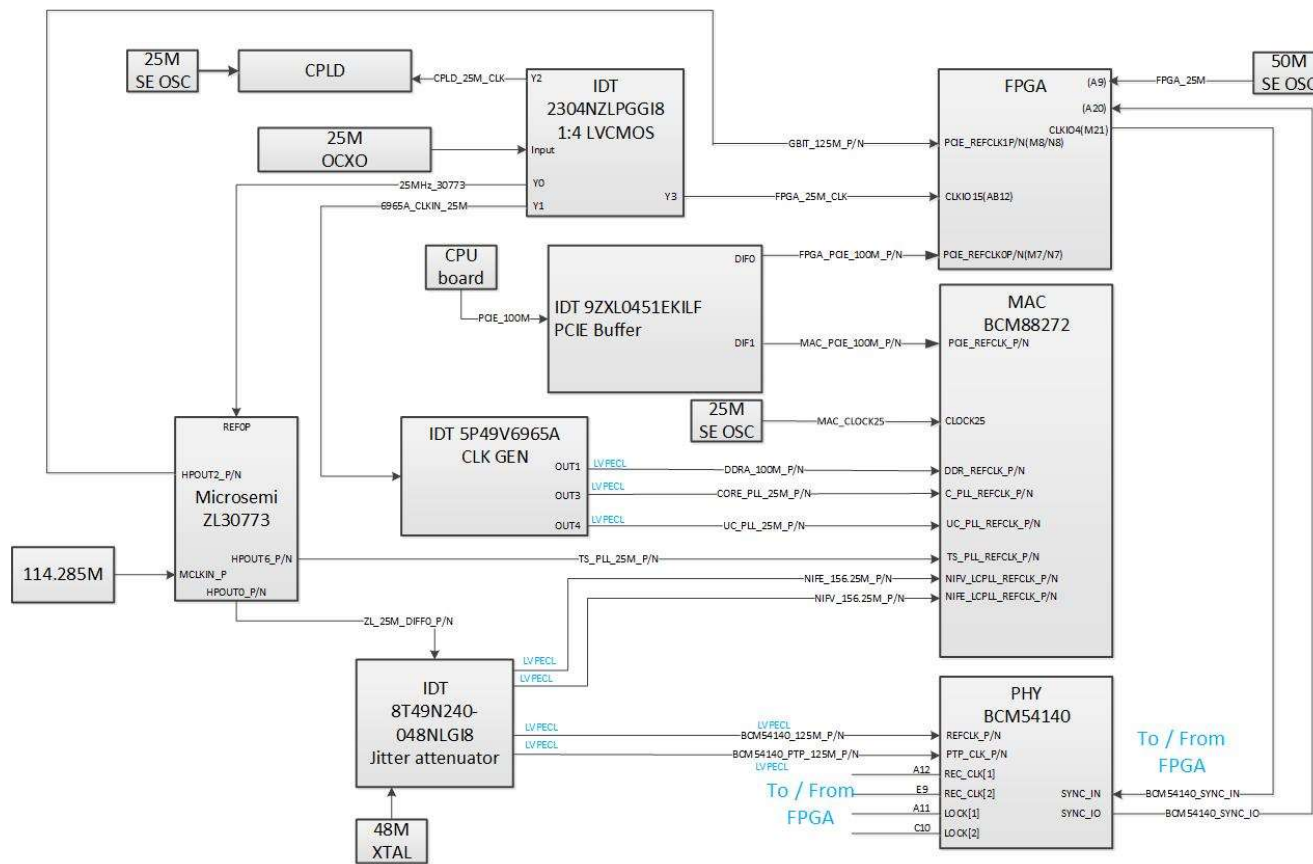
R0A board revision

2020-02-05

By: Heimdall Siao



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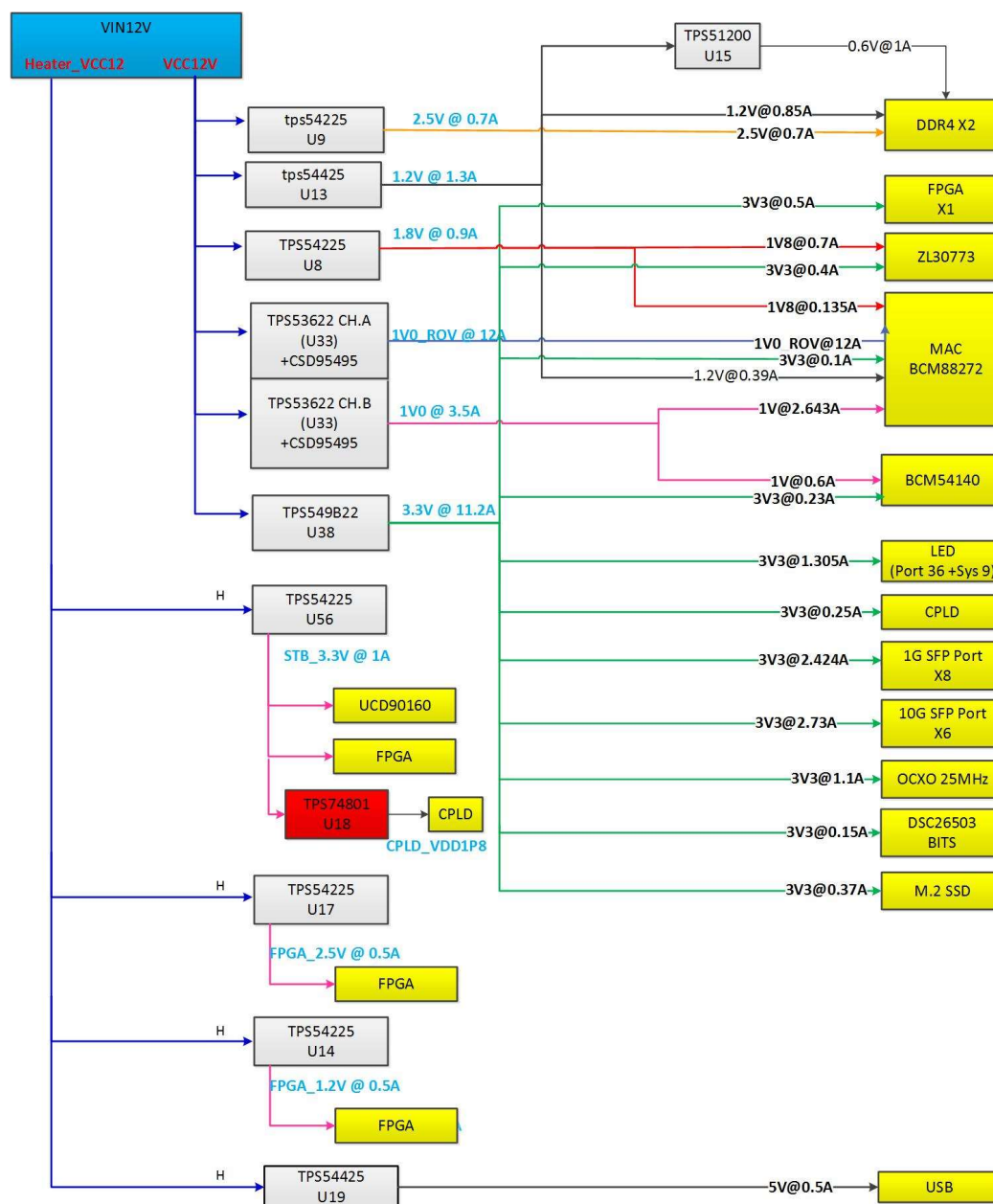


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Model Name	AS9915-18X	Rev	R0A
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Power Consumption Estimation Table														
Voltage(V) Device	12	5	3.3	standby	3.3	1.8	1.8	2.5	2.5	1.2	1.2	0.6	1	1
CPU Module is below														
all of CPU module														36.00
Main Board is below														
Broadcom BCM88272			0.100		0.135						0.381		12.000	2.700
Broadcom BCM54140			0.223										0.599	1
DDR4														
Hynix H5AN4G6NAFR-UHI 256MX16								0.333			0.425	0.500		2
CPLD (Altera 5M22102F3241FW)			0.250			0.600								1
FPGA (Altera)				0.500				0.500	0.500					1
ZL30773			0.400		0.700									1
Clock			1.500											1
Maxim DS26503LN+ (BITS)			0.150											1
OCXO 25MHz (Rakon STP 2921 LF)			1.100											1
UCD90160				0.500										1
USB CONN & USB HUB		0.500	0.320											1
M.2 SSD			0.370											1
1G_SFP Port			0.303											8
10G_SFPx Port			1.060											6
Fan Tray														
Fans	1.500													4
Other		0.500												
SFPxSFP LEDs			0.030											36
SYS LEDs			0.025											9
Total Current(A)	6.000	1.000	13.000	1.000	0.835	0.600	0.700	0.500	0.500	1.250	1.000	12.000	3.299	
														119
FSU Efficiency(90%)													Total Power(Efficiency(90%))	132

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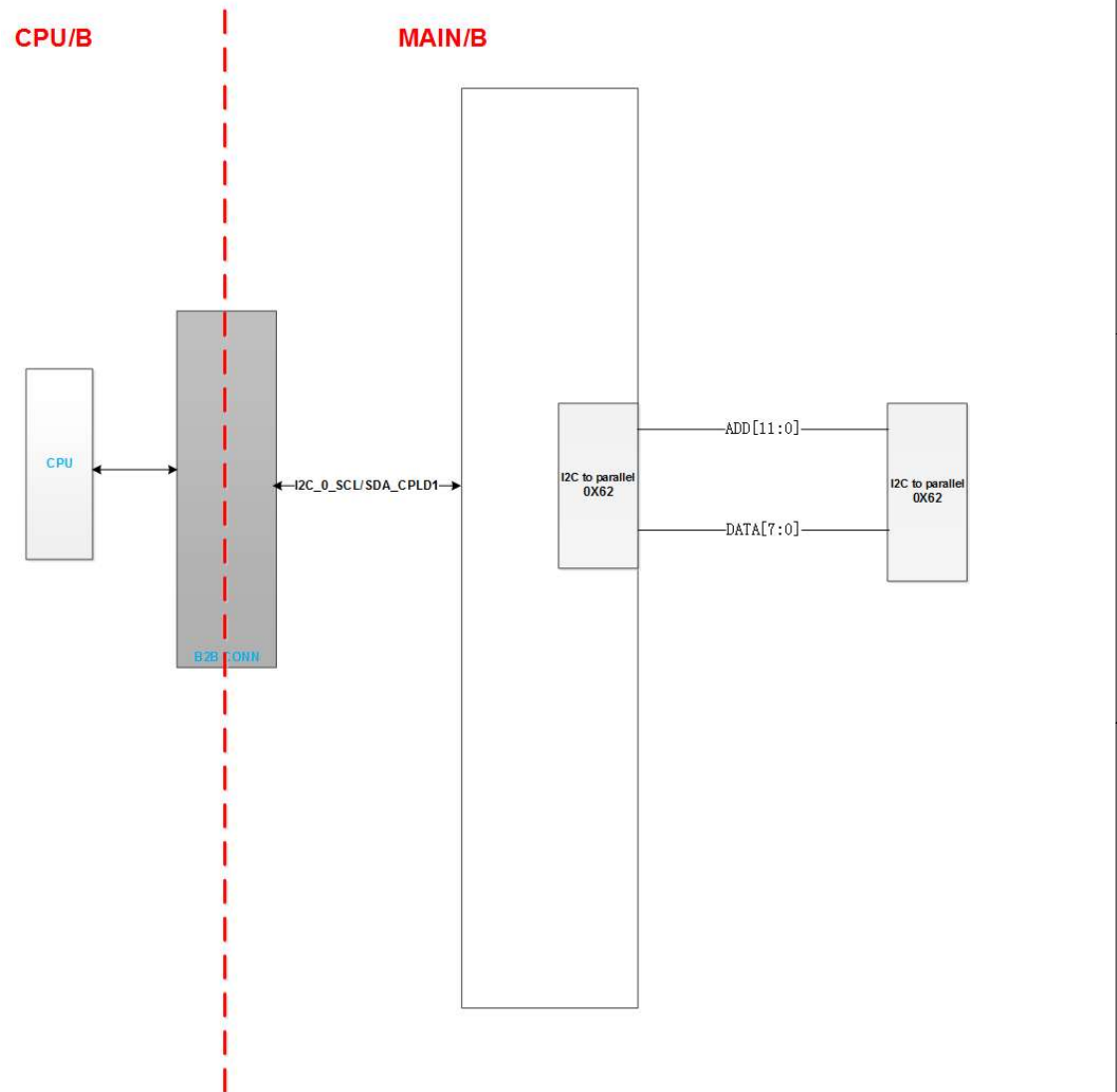
Model Name		AS5915-18X	Rev	R0A
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C	P007_Power Consumption	daniel		
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FMA-HW01008-01 R01

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Model Name		AS5915-16X		Rev	R0A
Page Name	P008_Reset Diagram			Engineer	Jarvis
Custom					
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AS5915-18X

Rev

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Size

Custom

Page Name

P012_JTAG Diagram

Engineer

Jamei

Date:

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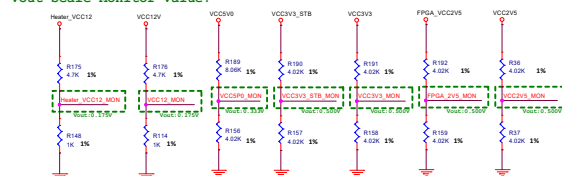
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Model Name		R0A
AS5915-18X		
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D	P013_1588 SyncE Dis	gammal
Ver	Wednesday, January 20, 2010	11:30 AM

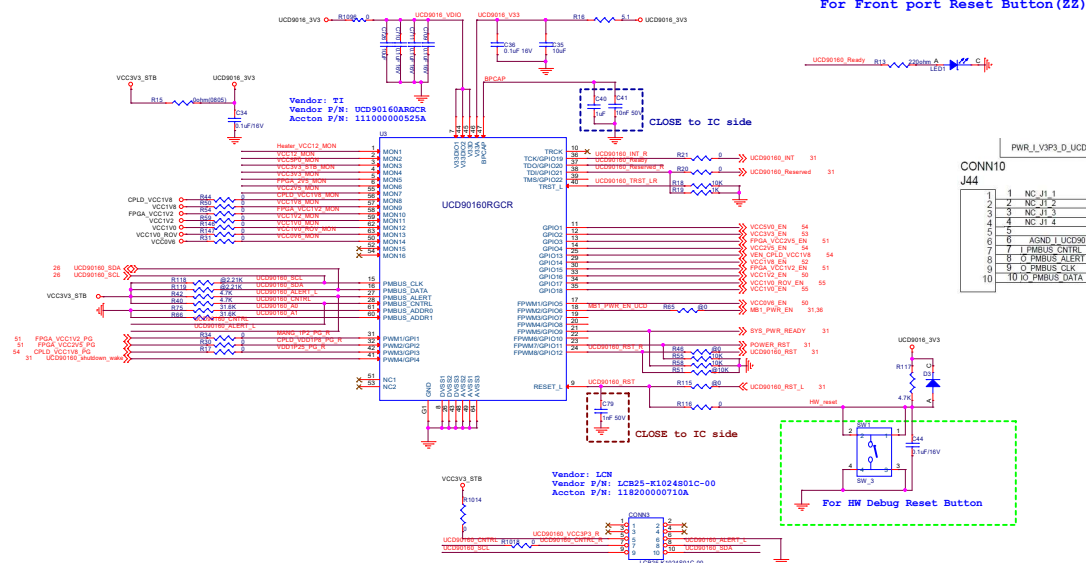
Vout Scale Monitor Value:



Note:
If the vout is under "2.5V", the
"vout scale monitor value" is
only to set 1V. So these voltage
are not divided across two series
resistors.

Put close to UCD90160

VCC12_MON	C74	0.1uF 10V
VCC1V_MON	C85	0.1uF 10V
VCC0V5_MON	C75	0.1uF 10V
VCC3V3_STB_MON	C76	0.1uF 10V
VCC0V3_MON	C77	0.1uF 10V
FPGA_VCC0V5_MON	C78	0.1uF 10V
VCC0V5_MON	C46	0.1uF 10V
CPLD_VCC0V5_MON	C50	0.1uF 10V
VCC1V8_MON	C58	0.1uF 10V
VCC1V8_MON	C58	0.1uF 10V
FPGA_VCC1V8_MON	C60	0.1uF 10V
VCC1V8_MON	C61	0.1uF 10V
VCC1V8_MON	C72	0.1uF 10V
VCC1V8_MON	C73	0.1uF 10V
VCC1V8_MON	C43	0.1uF 10V

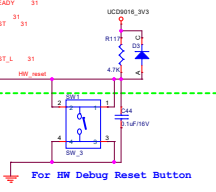


For Front port Reset Button (ZZ)

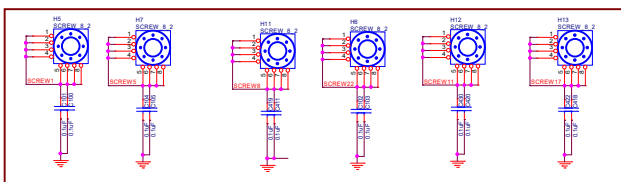


CONN10 J44

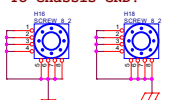
1	NC J1 1
2	NC J1 2
3	NC J1 3
4	NC J1 4
5	
6	AGND 1 UCD90160
7	PMBUS_CTRL
8	PMBUS_ALERT
9	PMBUS_CLK
10	TO PMBUS DATA



Mounting Hole



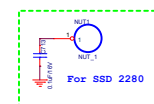
To chassis GND.



A-Type Screw



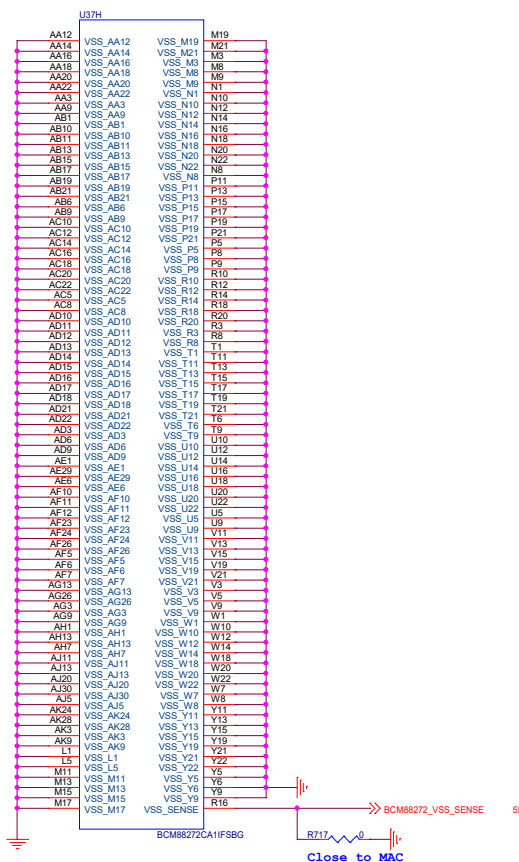
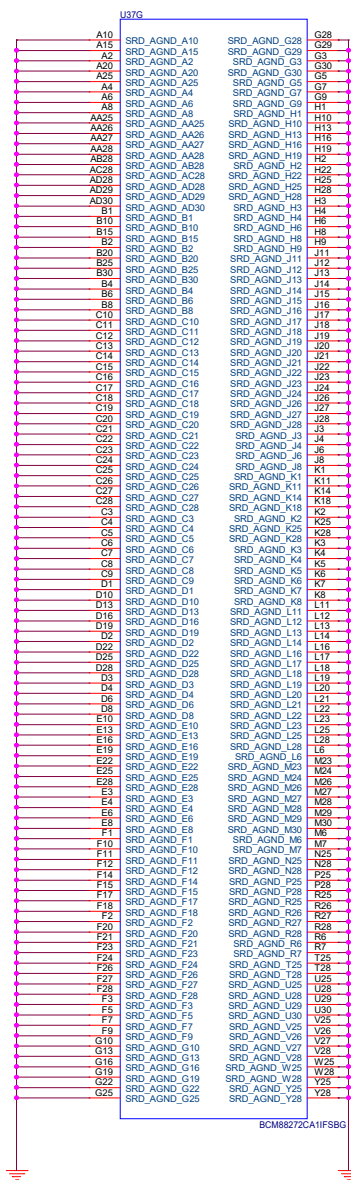
For SSD 2242



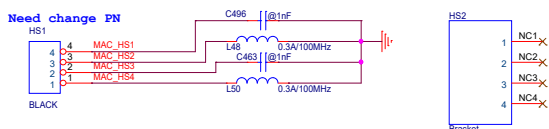
For SSD 2280

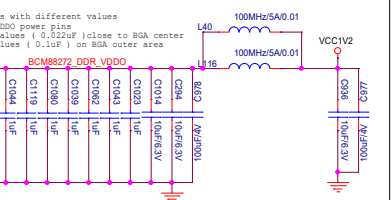
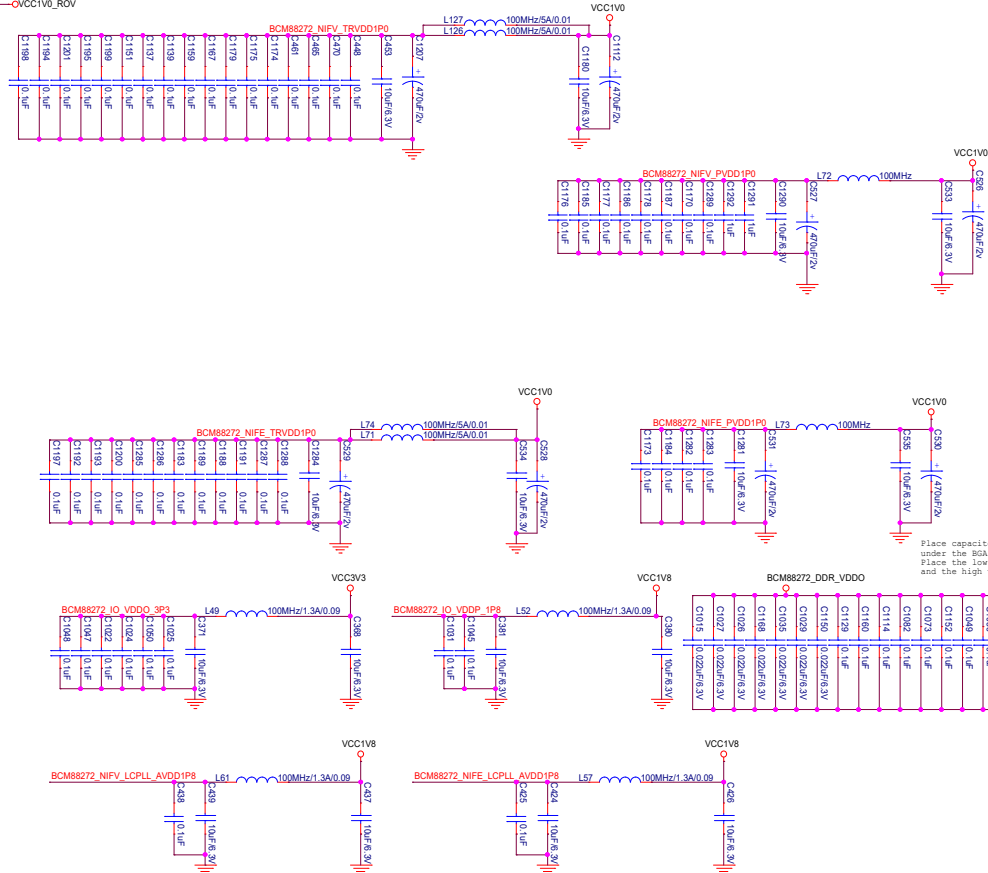
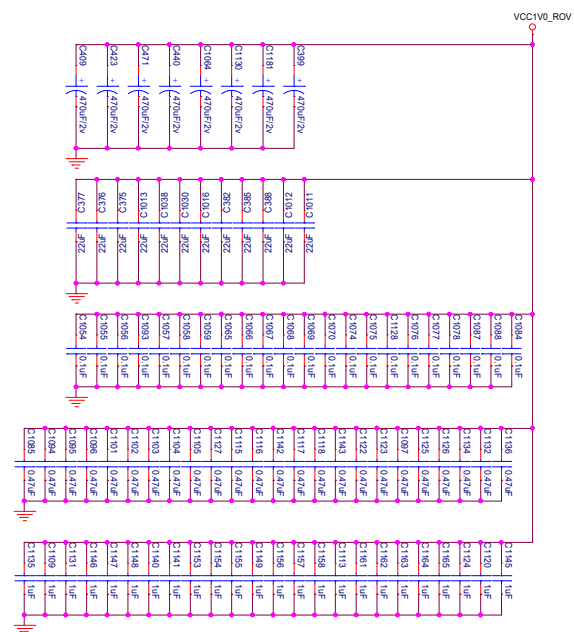
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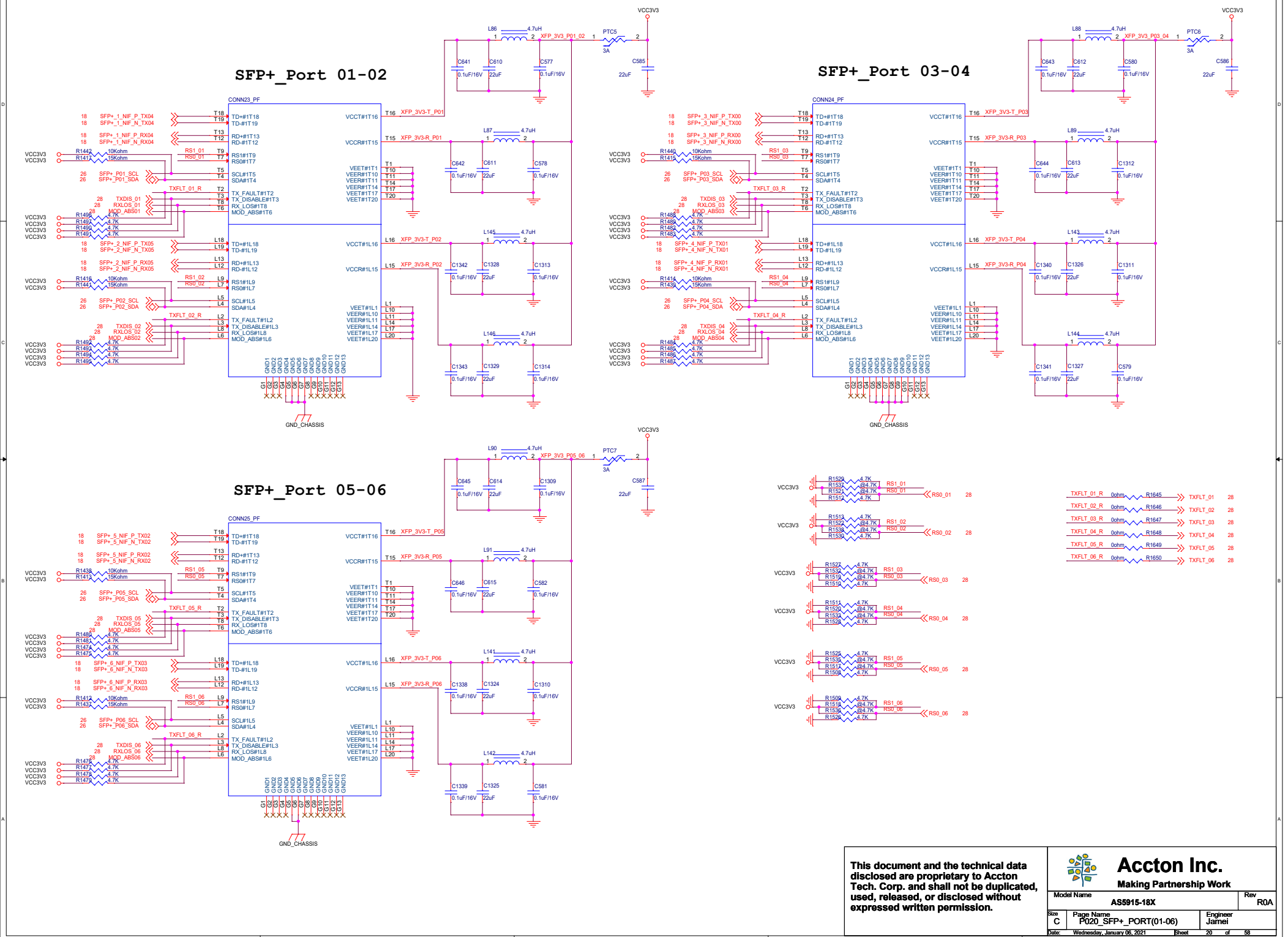
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Model Name	AS915-18X	Rev	R0A
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Note: All of the device's analog and digital grounds **must** be tied together at the board level to the same single ground. The core decoupling capacitors should be located between VDDC and VSS vias and not on AGND vias, even though AGND and VSS are shorted on the board level. The same rule should be applied for all digital rails such as VDDQ_3P3 and IO_VDDP_1P8 for keeping AGND clean from IO and Core rails.





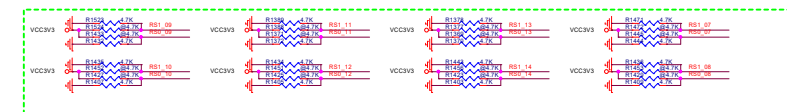
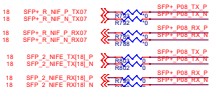


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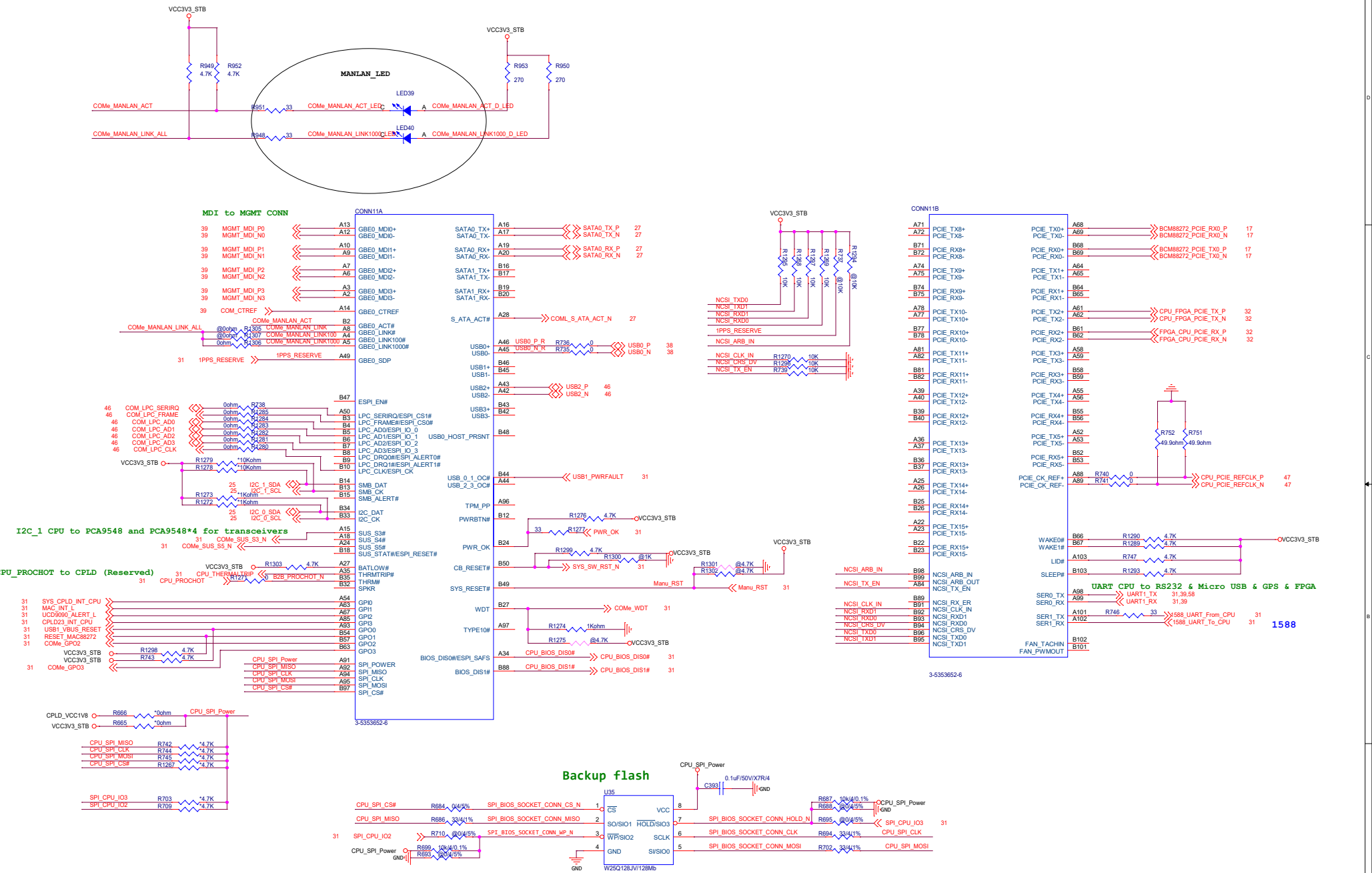


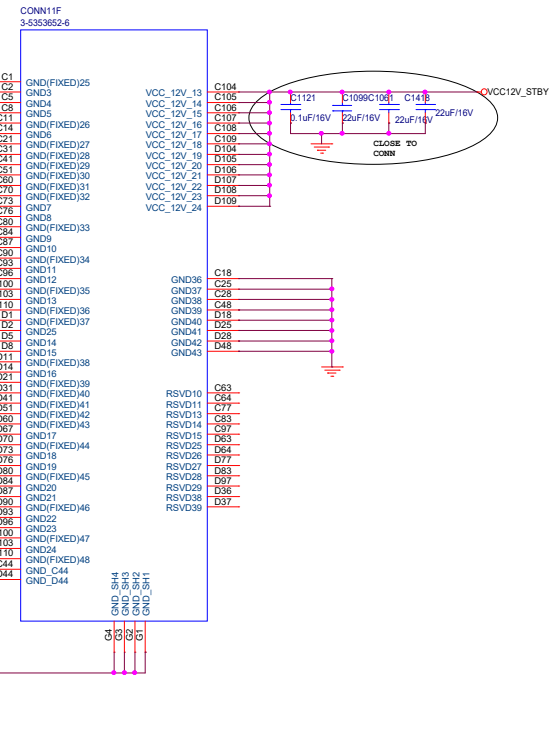
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Model Name		AS5915-18X	Rev	R0A
Size	Page Name	P020_SFP+_PORT(01-06)	Engineer	Jamel
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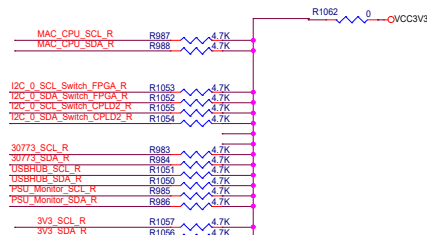
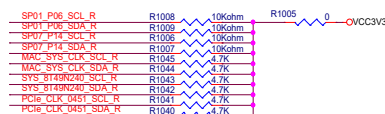
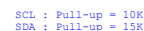


 Accton Inc. Making Partnership Work		Rev	
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AS5915-18X			
Size	Page Name	Engineer	
D	P021_SFP_PORT(07-14)	Jamei	
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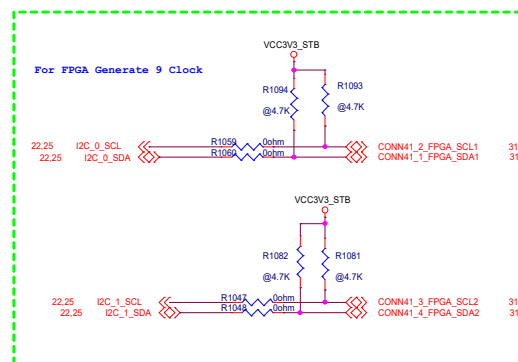
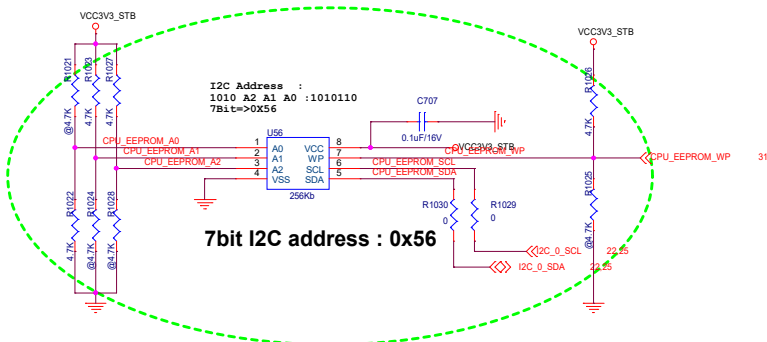




Model Name		AS5915-18X		Rev		ROA	
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C	P024_cornE_3			Jamei			
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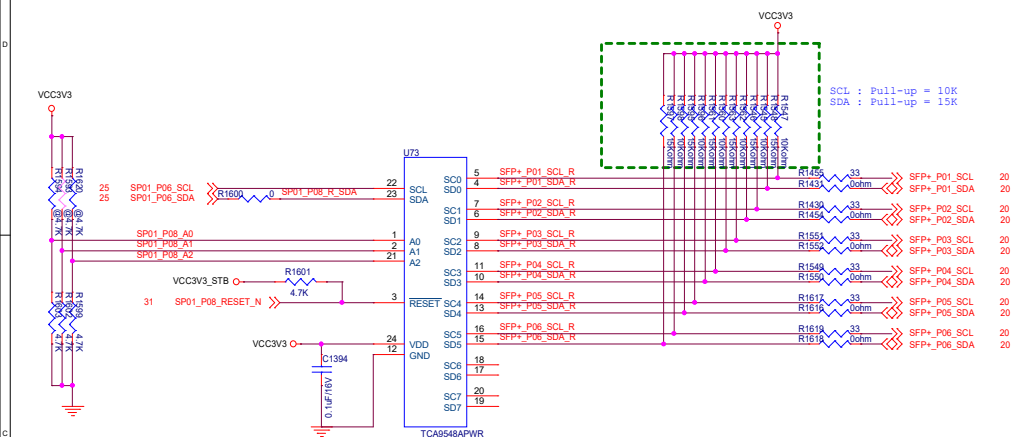


Note:
I2C Address:
1110 A2 A1 A0 : 1110110 7bit I2C address : 0x76
7Bit => 0x76

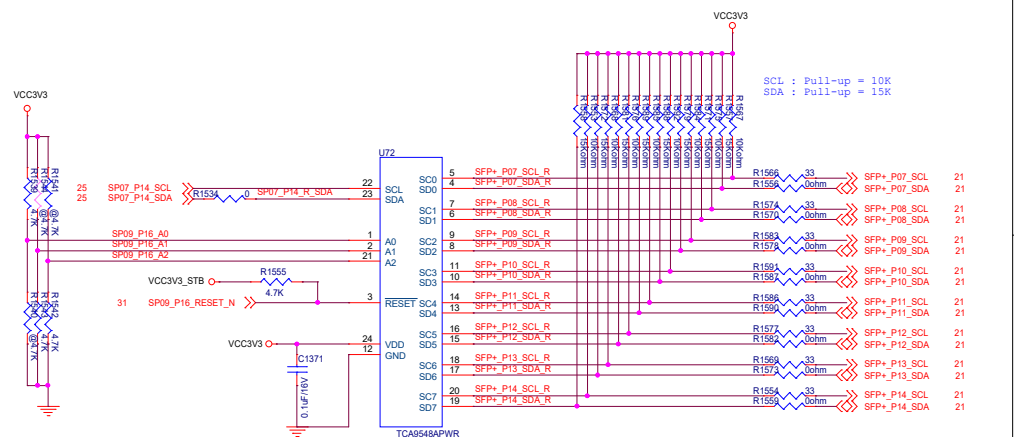


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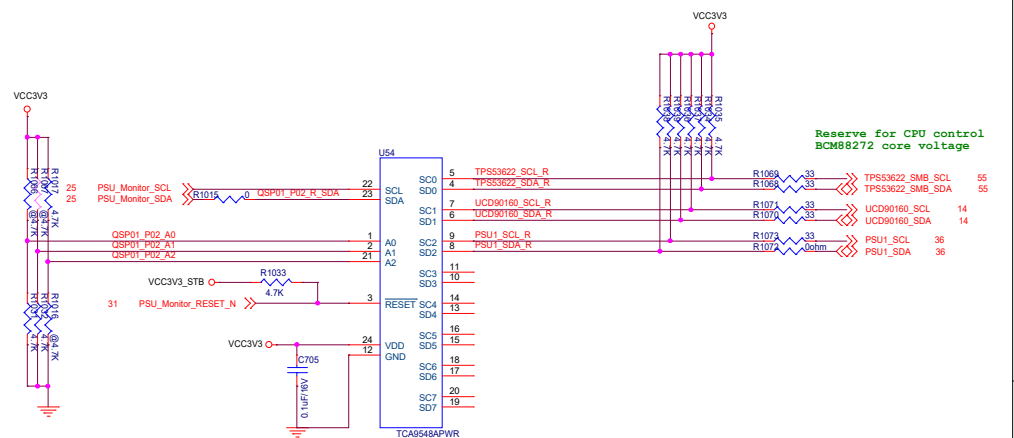
I2C LEVEL-1 TO I2C LEVEL-2



Note:
I2C Address:
1110 A2 A1 A0 : 1110000 7bit I2C address : 0x70
7Bit => 0x70



Note:
I2C Address:
1110 A2 A1 A0 : 1110001 7bit I2C address : 0x71
7Bit => 0x71



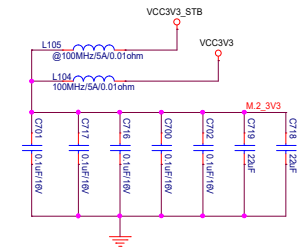
Note:
I2C Address:
1110 A2 A1 A0 : 1110100 7bit I2C address : 0x74
7Bit => 0x74

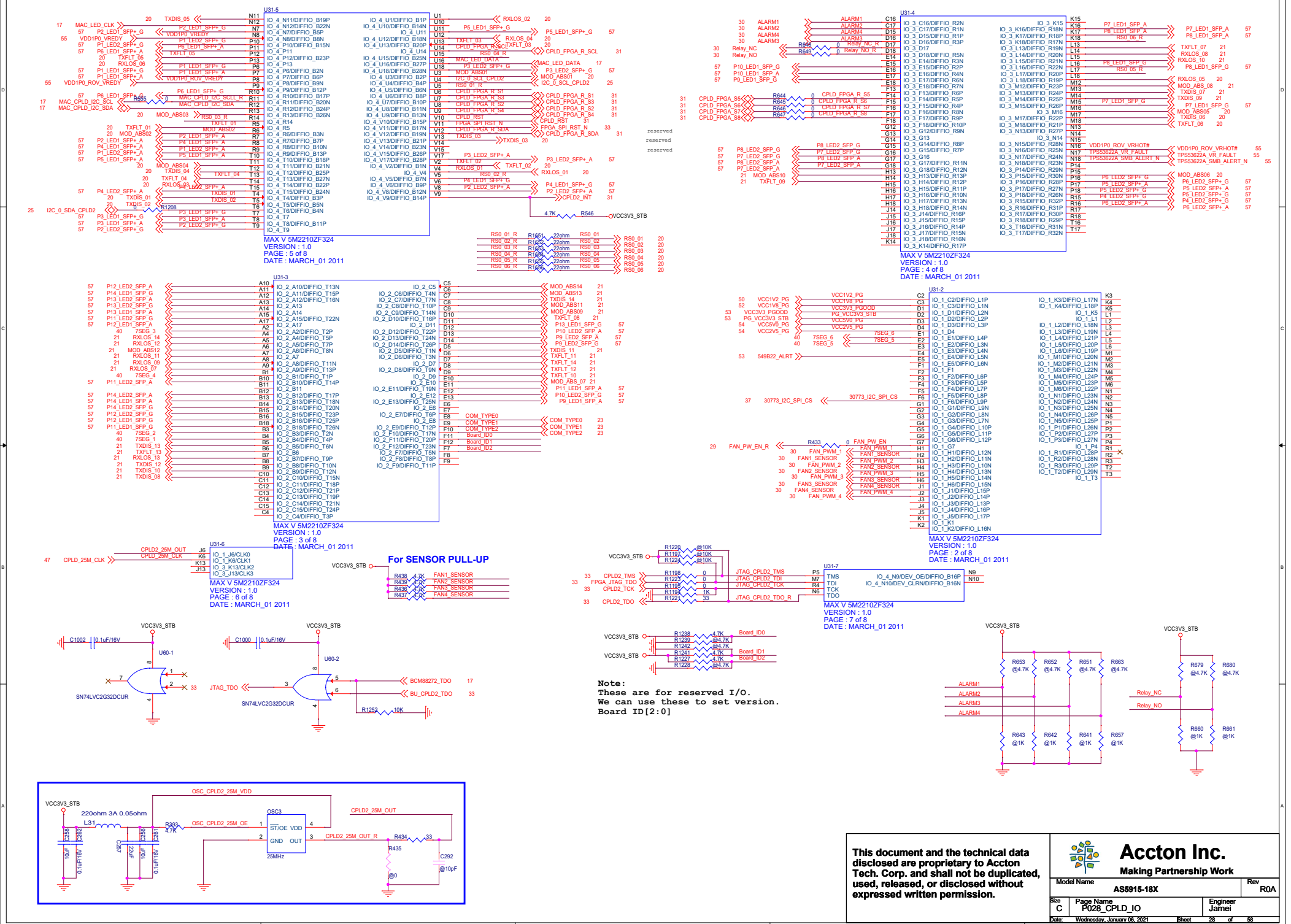
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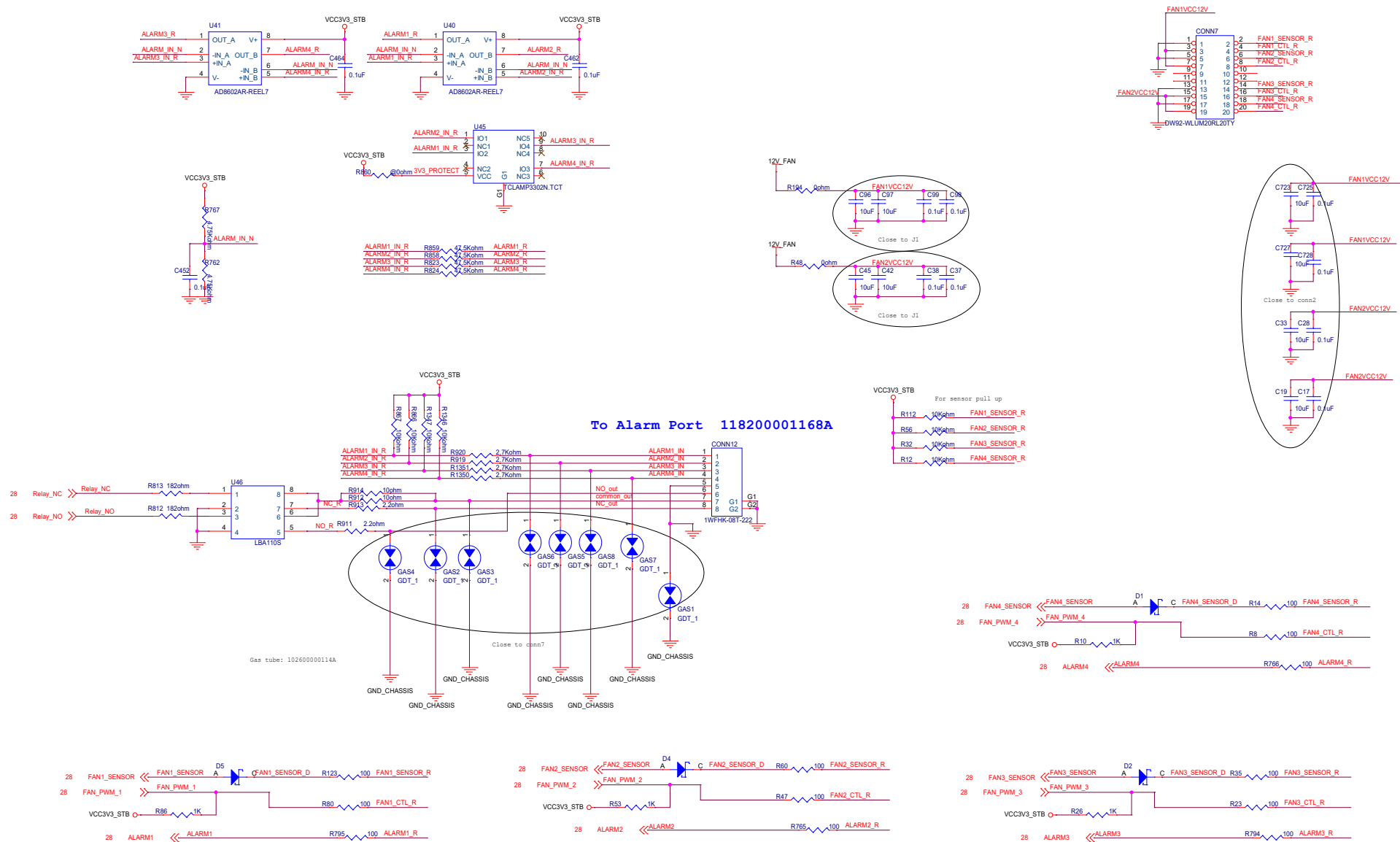
Model Name	AS5915-18X	Rev	R0A
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C	P026_I2C_Switch_PCA9548	Jamel	
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C	P029 CPLD IO POWER			Jamei			
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Model Name	AS5915-18X	Rev	R0A
Size	C	Page Name	P030_ALARM / Fan Control
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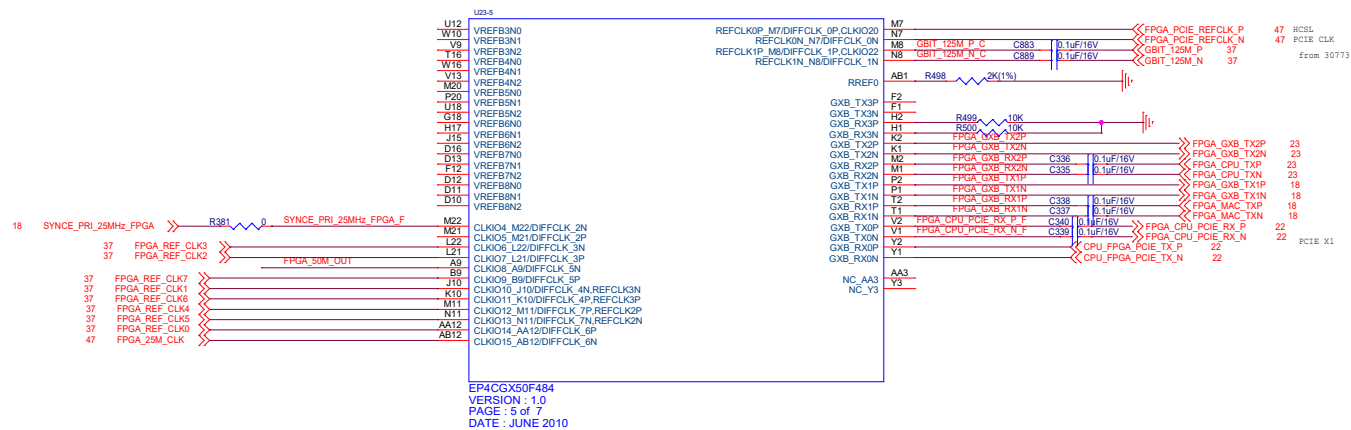
(07/27) Note:
-> FPGA(U13) I/O(U13)
For LED stream signal enable => when
MAC reset is high



```
Note:
These are for reserved I/O.
We can use these to set version.
Version ID[3:1]>= PCB_Ver_3 , PCB_Ver_2 , PCB_Ver_1
R001 : ROA
010 : ROB
011 : ROC
100 : ROD
101 : ROE
110 : RO1
others:reserved
```



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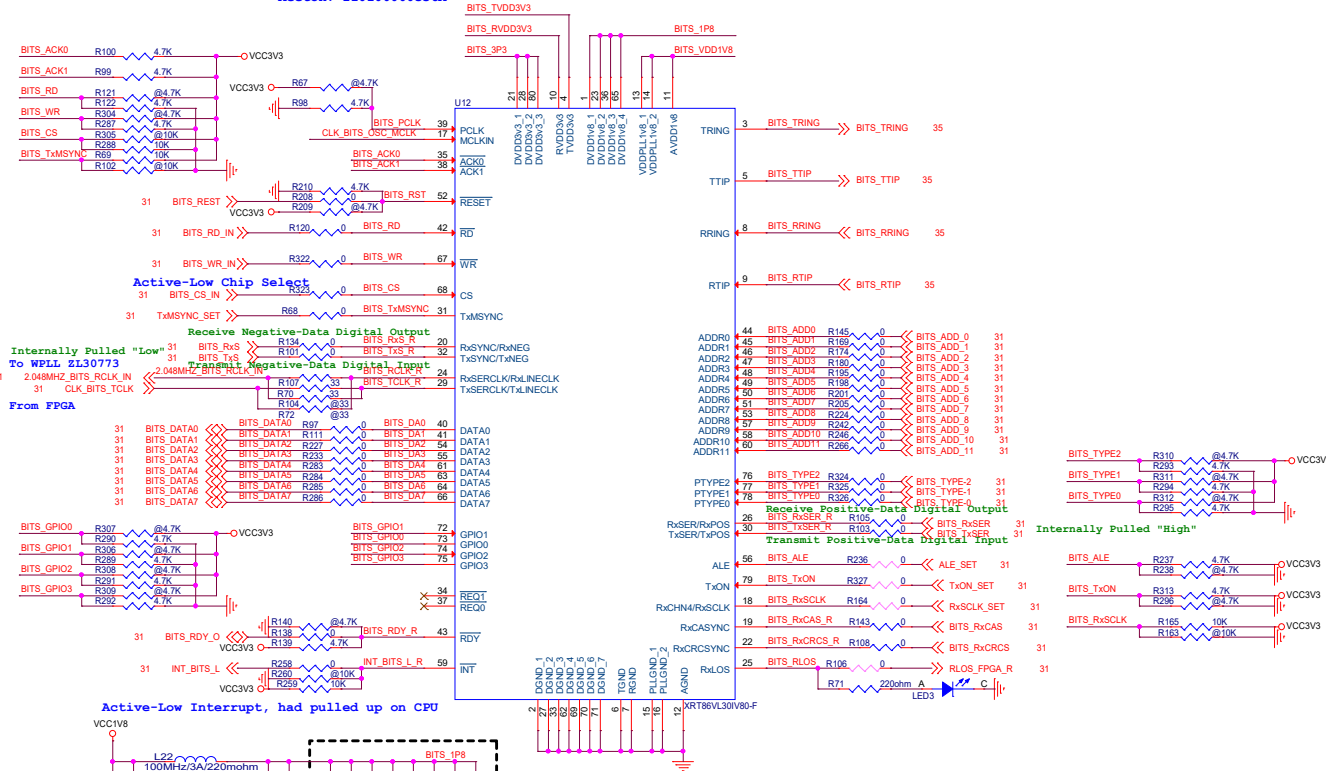


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Model Name		AS5915-18X	Rev	R0A
Size	Page Name	P032_FPGA_CLOCK	Engineer	Jameli
C				
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Ext Clock XRT86VL30IV80-F

Vendor: EXAR
P/N: XRT86VL30IV80-F
Accton: 110100000556A



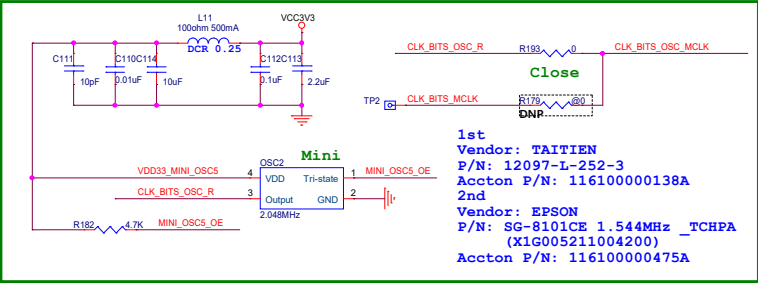
OPERATION MODE	FREQUENCY OF TXINCLK0(MHz)
2.048MVIP non-multiplexed	2.048
4.096MHz non-multiplexed	4.096
8.192MHz non-multiplexed	8.192
12.352MHz Bit-multiplexed (DS1 ONLY)	12.352
16.384MHz Bit-multiplexed	16.384
16.384 HMVIP Byte-multiplexed	16.384
16.384 H.100 Byte-multiplexed	16.384

Microprocessor Type Input:
These input pins permit the user to specify which type of Microprocessor/ Microcontroller to be interfaced to the XRT86VL30 device. The following table presents the three different microprocessor types that the XRT86VL30 supports.

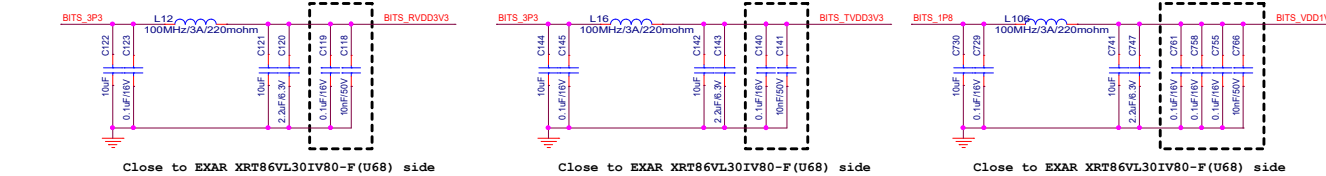
°PType2	°PType1	°PType0	MICROPROCESSOR TYPE
0	0	0	Intel Asynchronous
0	0	1	Motorola Asynchronous
1	0	1	IBM POWER PC 403

NOTE: These pins are internally pulled "Low"

P2 Change
Have the 2.048MHz Clock for XRT86VL30IV80-F MCLK



1st
Vendor: TAITIEN
P/N: 12097-L-252-3
Accton P/N: 116100000138A
2nd
Vendor: EPSON
P/N: SG-8101CE 1.544MHz_TCHPA
(X1G005211004200)
Accton P/N: 116100000475A



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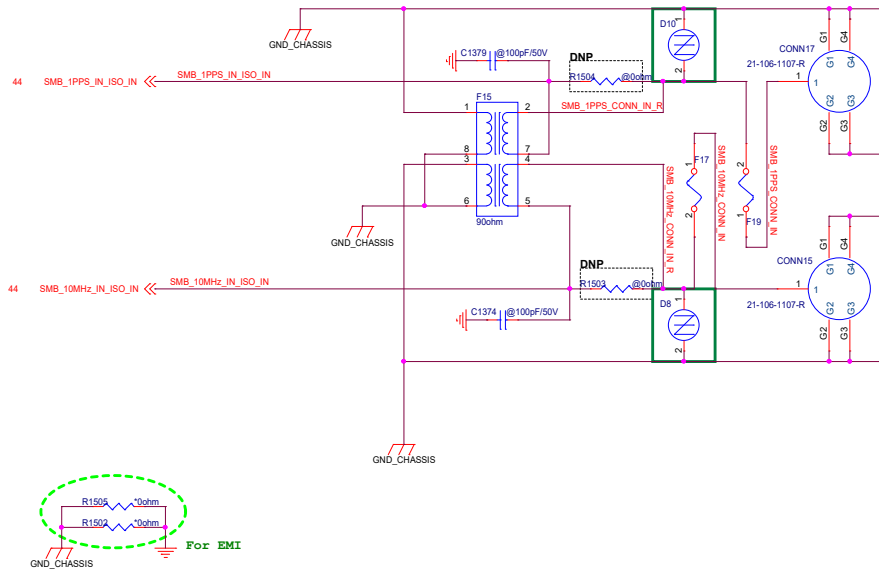


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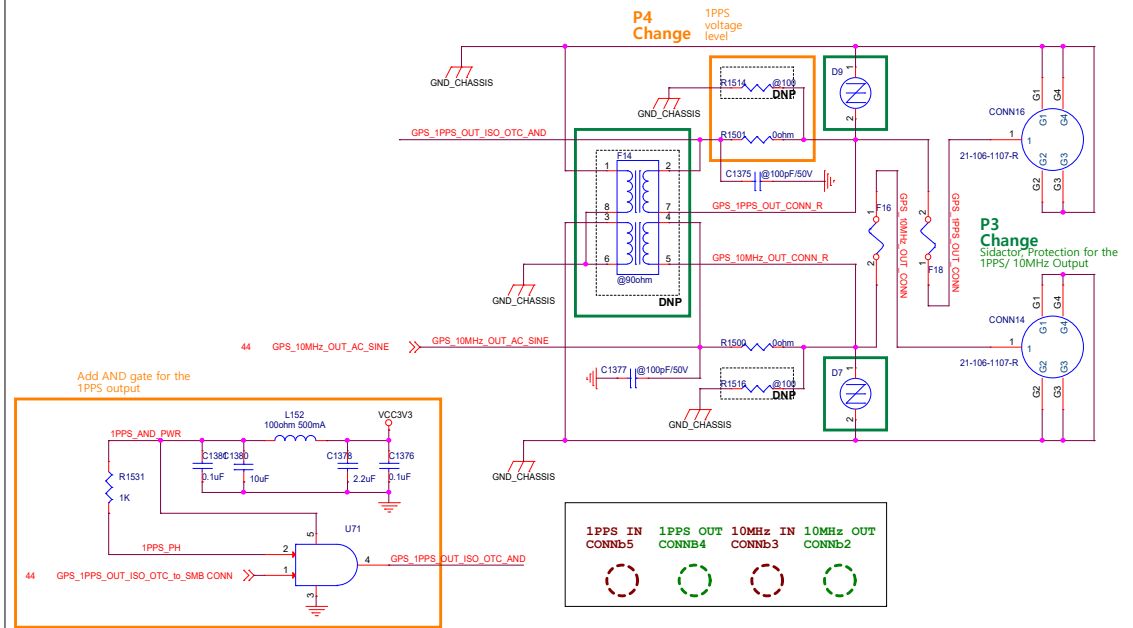
Model Name	AS5915-18X	Rev	R0A
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C	P034_TIMING_BITS_XRT86VL30IV80	80	
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GPS CONN

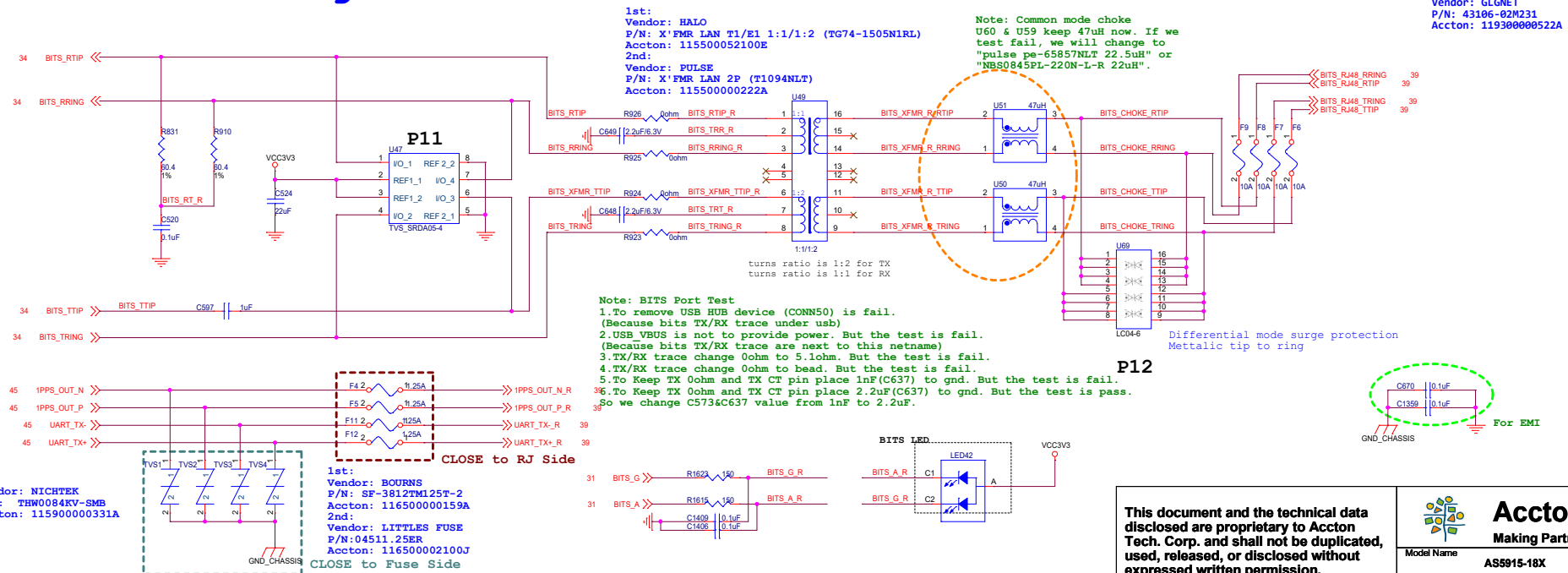
EXT_GPS_INPUT



GPS OUTPUT



External Timing Reference CONN

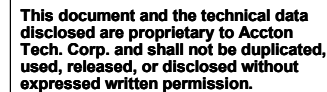


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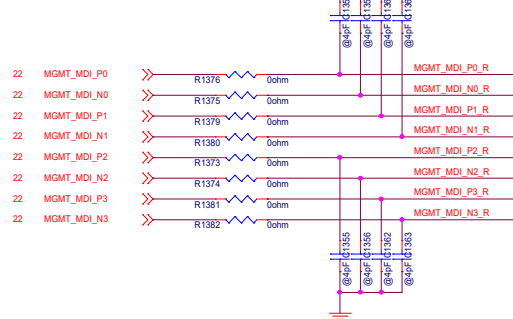
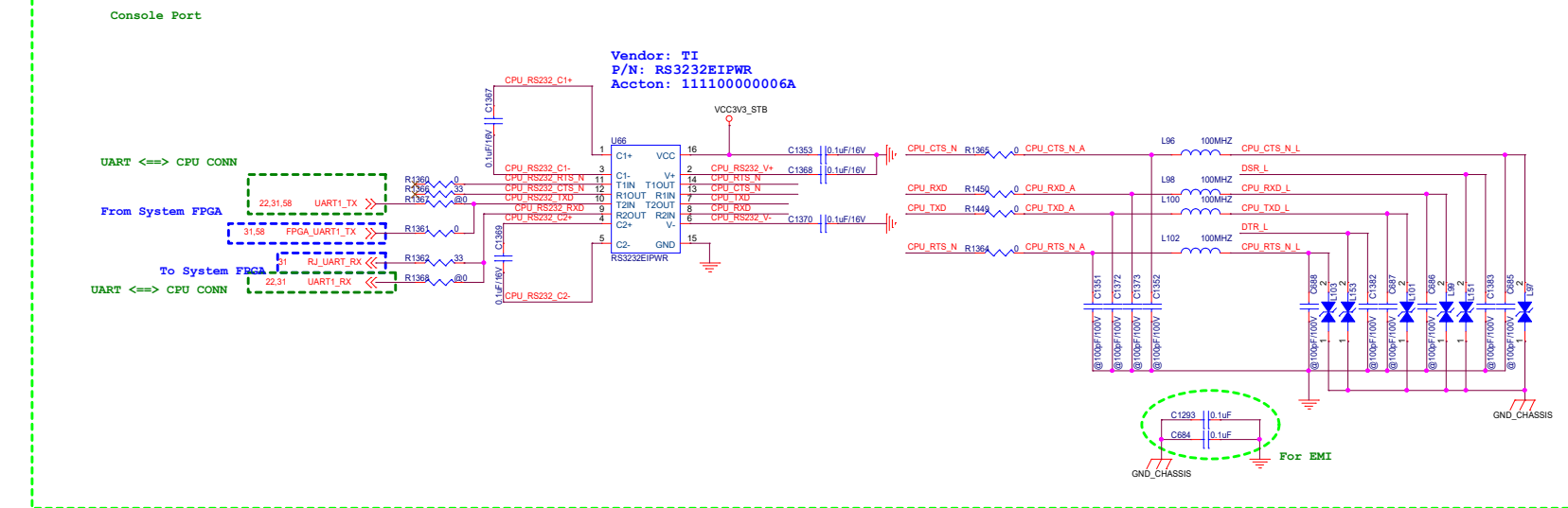


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Model Name		Rev
AS5915-18X		R0A
Size	Page Name	Engineer
C	P035_TIMING_GPS_EXT_CLK_CONN	Panel
Date:	Wednesday, January 06, 2021	Sheet 35 of 58

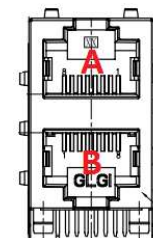
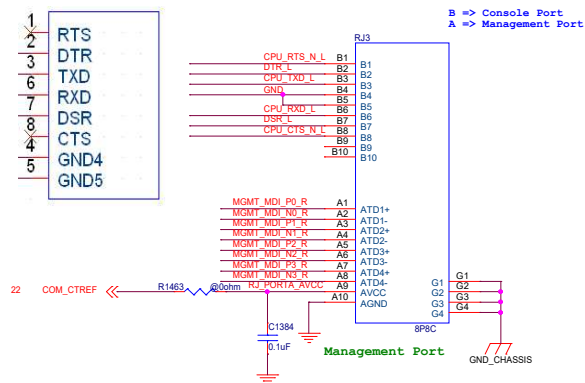
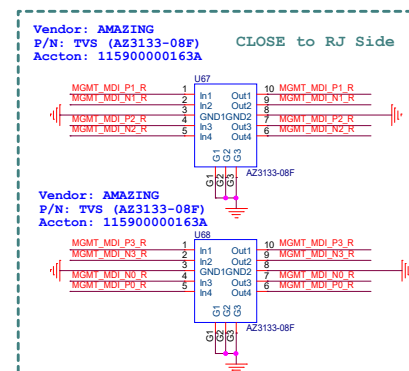
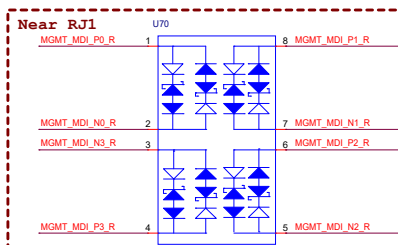


Model Name		AS5915-18X		Rev	R0
Size	Page Name	Engineer			
C	P038_USB Port_2.0 Type-A	Jamei			
Date:	Wednesday, January 06, 2021	Sheet	38	of	58

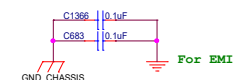
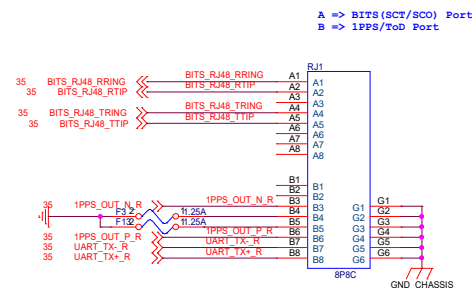


Path:
0ohm Res. -> U58 & U70 -> U69 -> RJ1

Vendor: BOURNS
P/N: TVS (CDNBS08-SLVU2.8-8)
Accton: 115900000018A
115900000018A 續料, 換1159000000302A



B => ToD Port
A => Bits Port



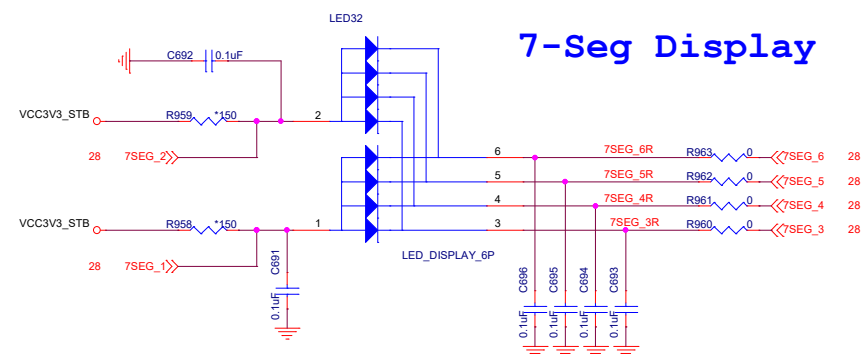
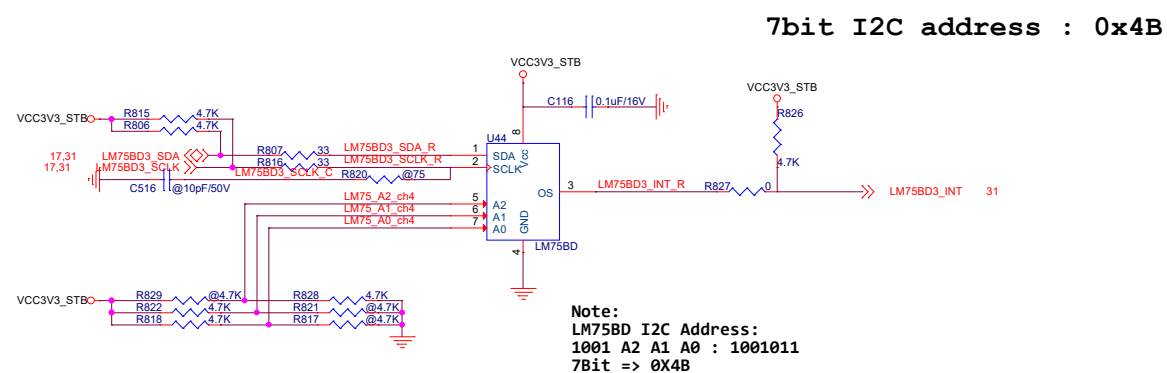
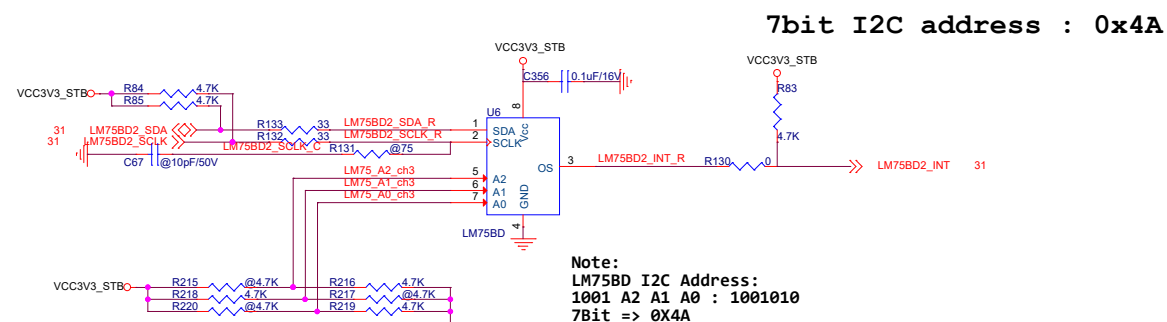
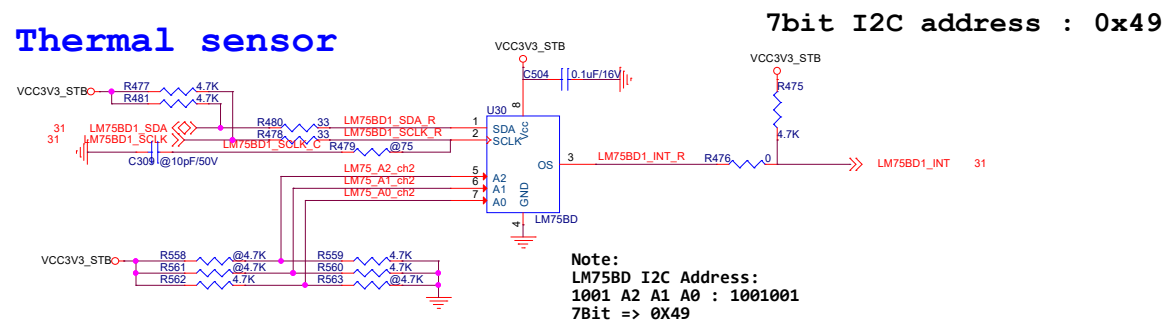
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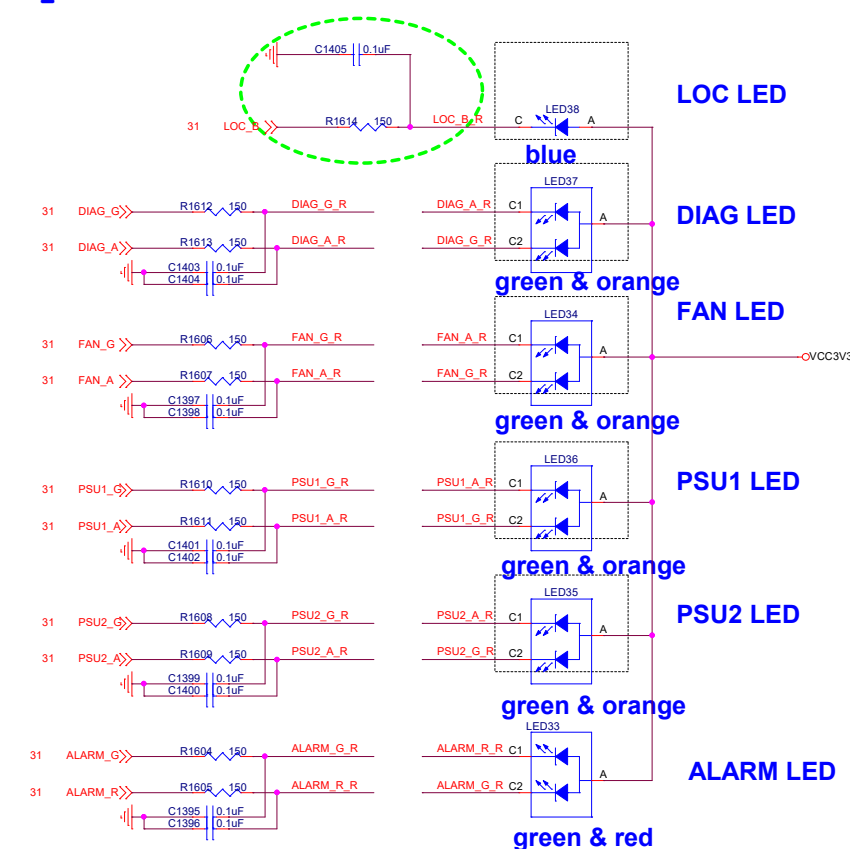
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Model Name		Rev
AS5915-18X		R0A
Size	Page Name	Engineer
C	P039_RJ Console & MGMT CONN	Jamel
Date	Wednesday, January 06, 2021	Sheet 39 of 58

Thermal sensor



System LED



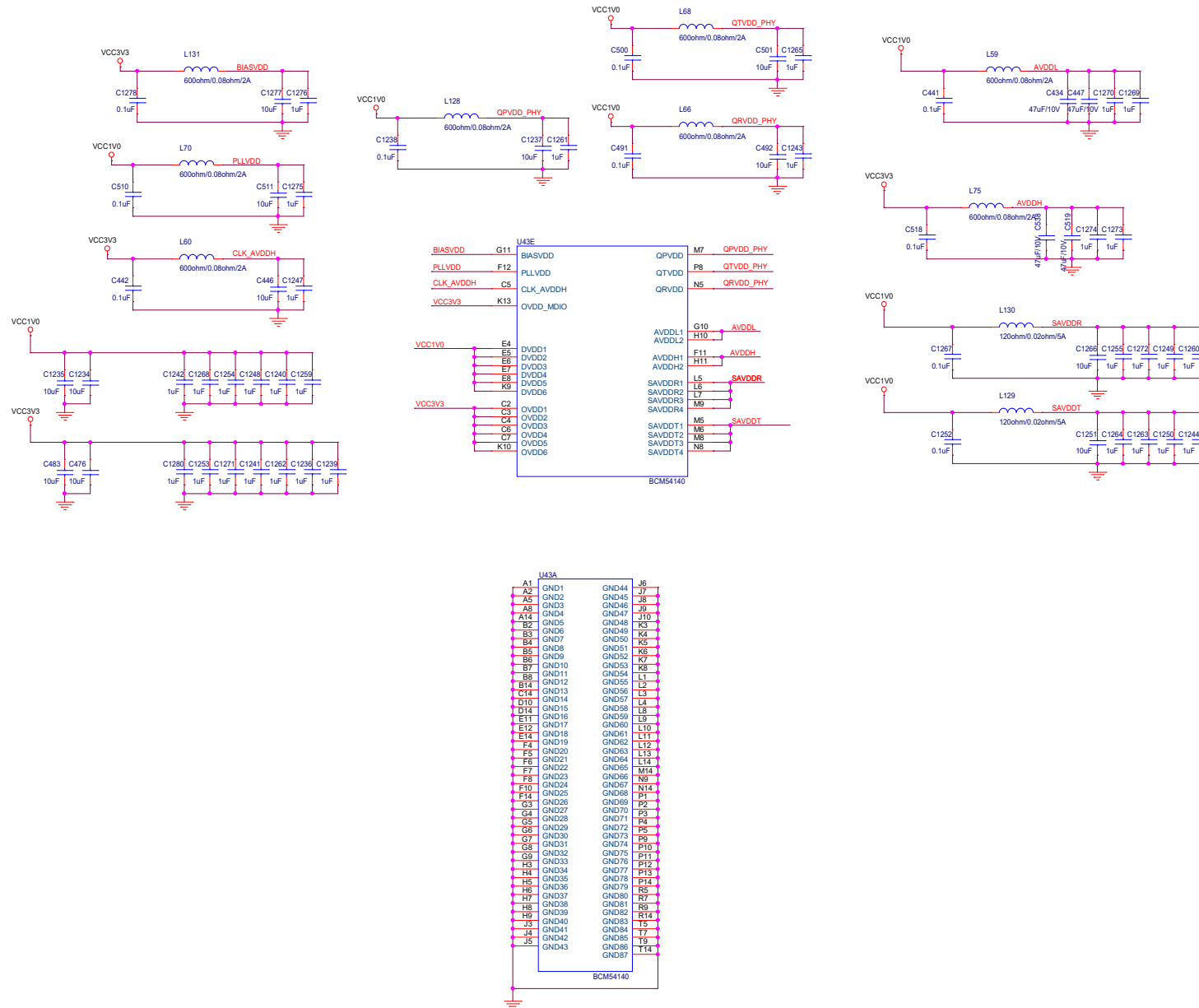
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Model Name	AS5915-18X		Rev	R0A
Size	Page Name	Engineer		
	CustomP040_LM75/SYS LED/7-SEG	Jamei		
Date:	Wednesday, January 06, 2021	Sheet	40	of 58

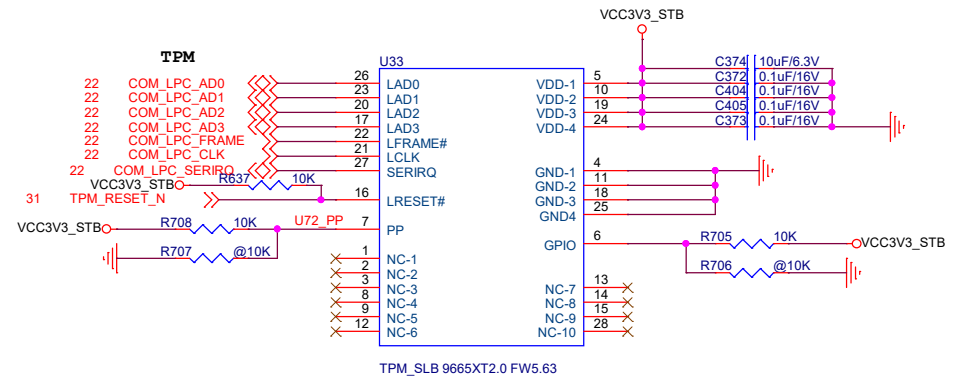
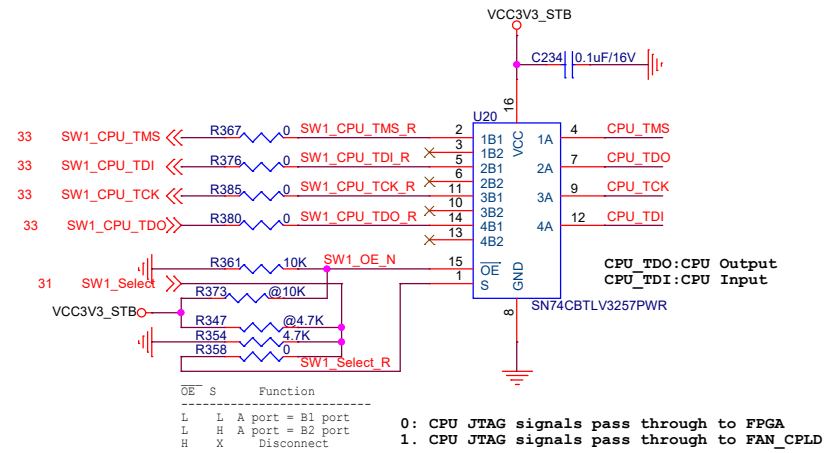
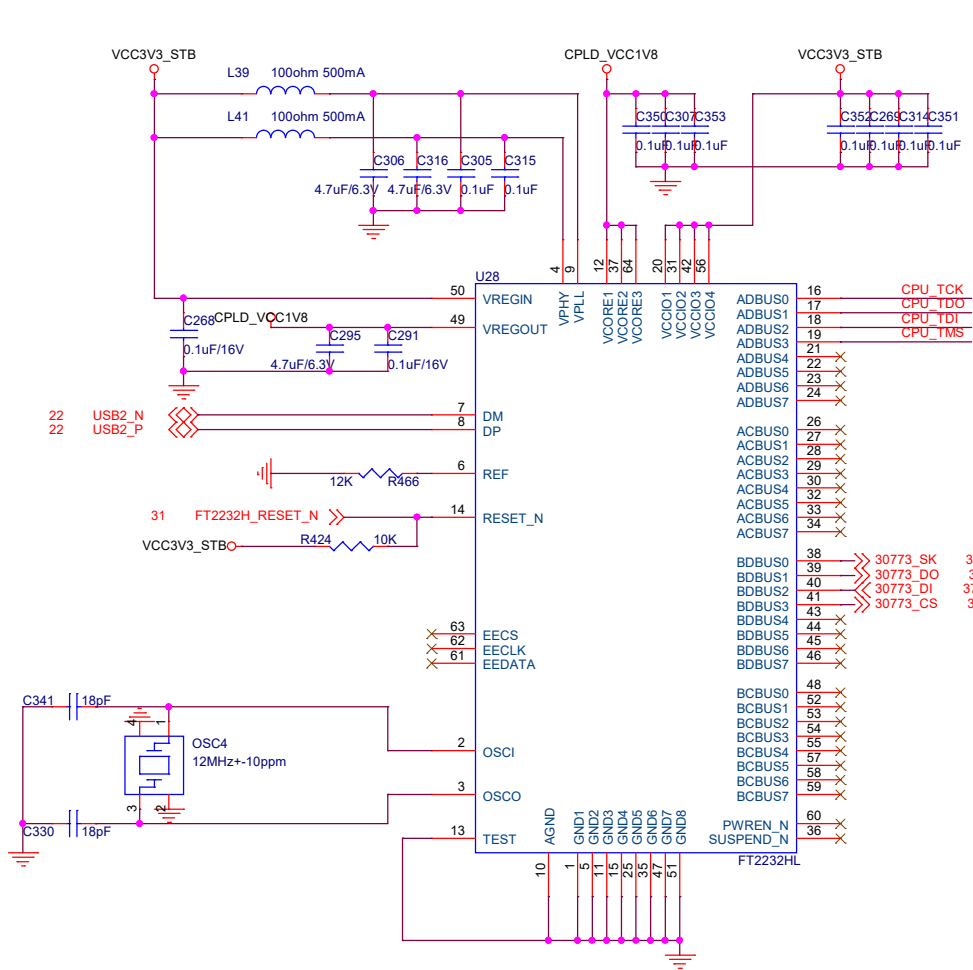


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Model Name	AS5915-18X	Rev	R0A
Size	C	Page Name	P042_PHY-54140_POW
Date	Wednesday, January 06, 2021	Sheet	42 of 58



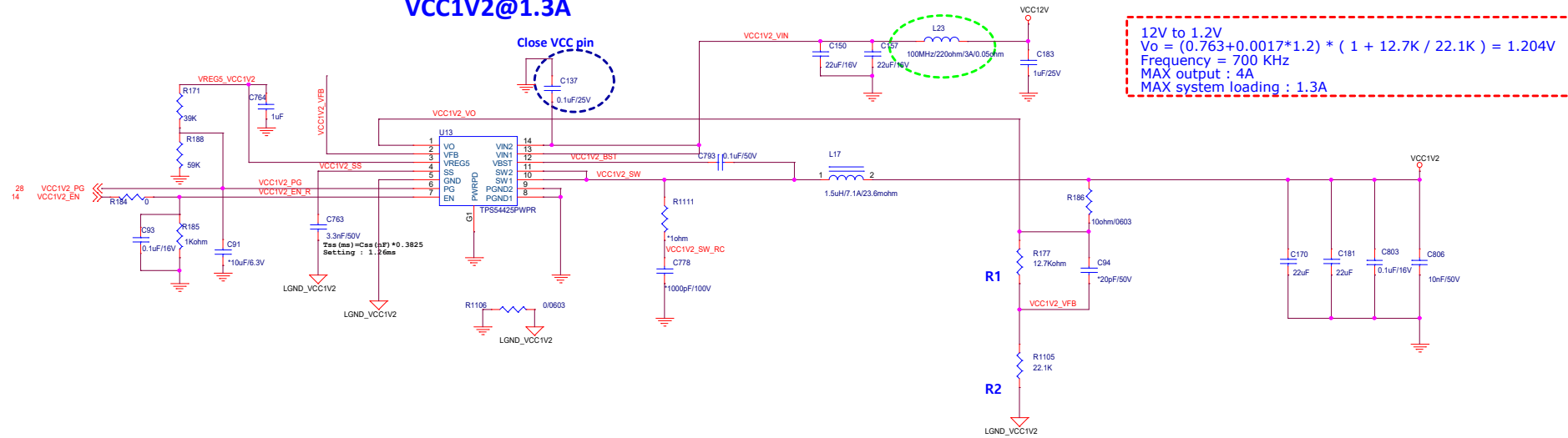
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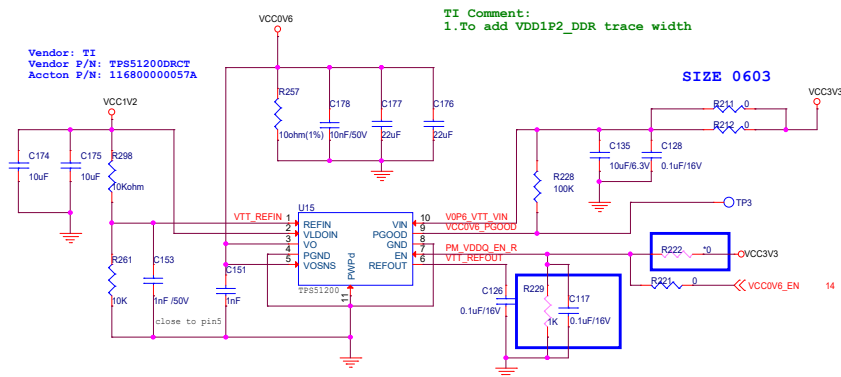
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Model Name		AS5915-18X	Rev	R0A
Size	Page Name	Engineer		
B	P046_USB_TO_JTAG & TPM	Jamei		
Date:	Wednesday, January 06, 2021	Sheet	46	of 58

VCC1V2@1.3A



VCC0V6/ 1A

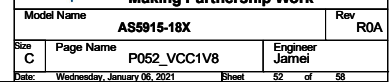


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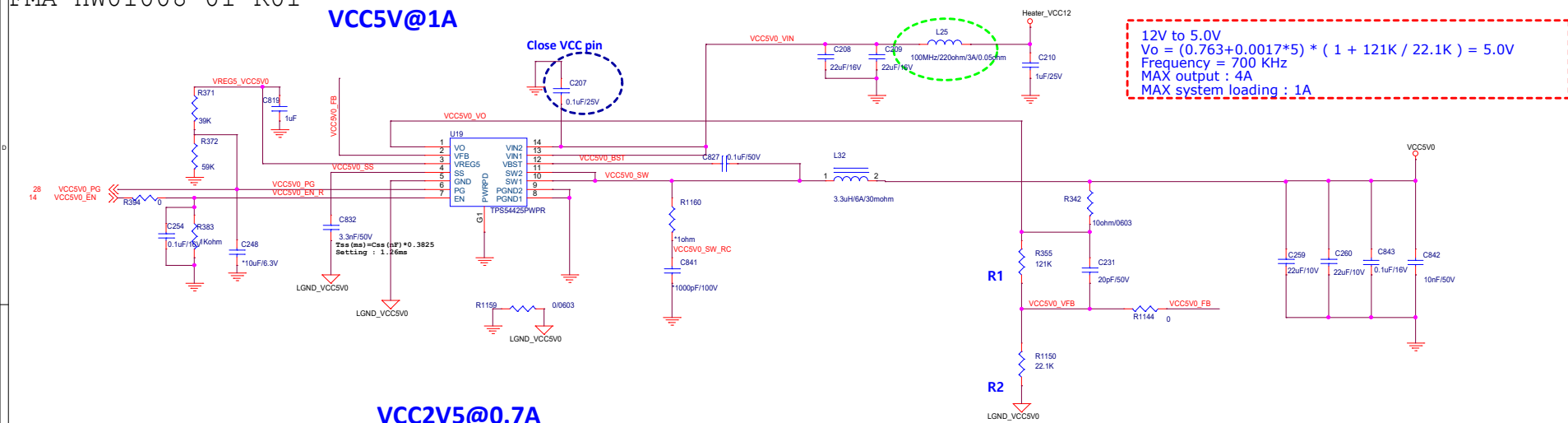


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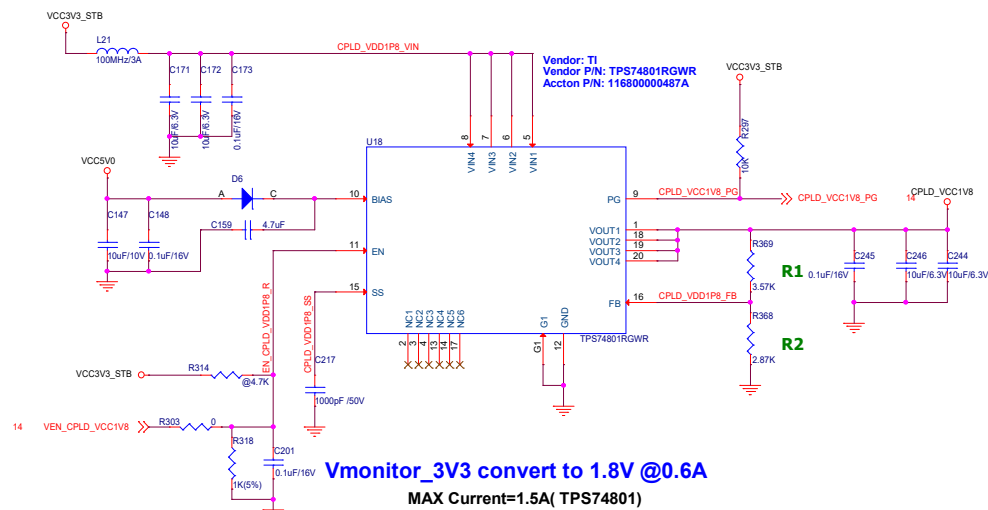
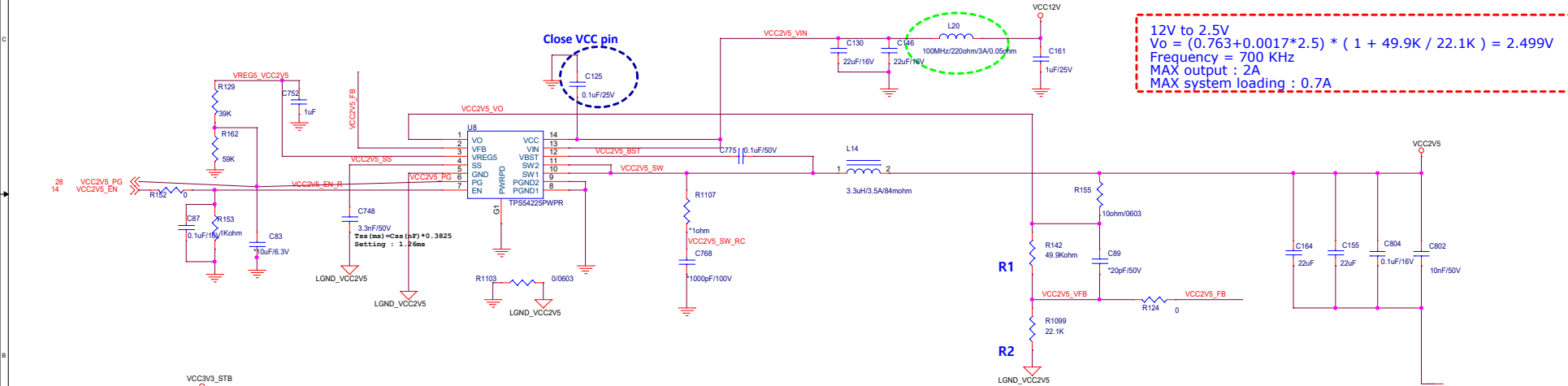
Model Name	AS5915-18X	Rev	R0A
Size	C	Page Name	P050_VCC1V2_VCC0V6
Date	Wednesday, January 06, 2021	Engineer	blamel
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VCC5V@1A



VCC2V5@0.7A

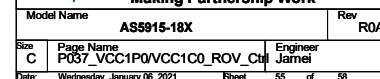


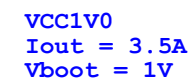
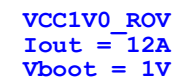
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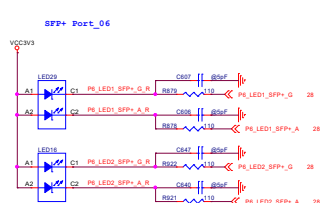
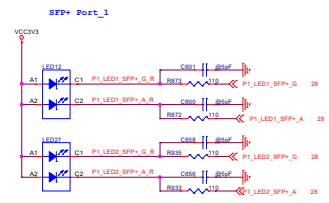
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Model Name	AS5915-18X	Rev	R0A
Size	Page Name	Engineer	Model
C	P054_VCC5V_VCC2V5_CPLD_VCC1V8		
Date	Wednesday, January 06, 2021	Sheet	54 of 58



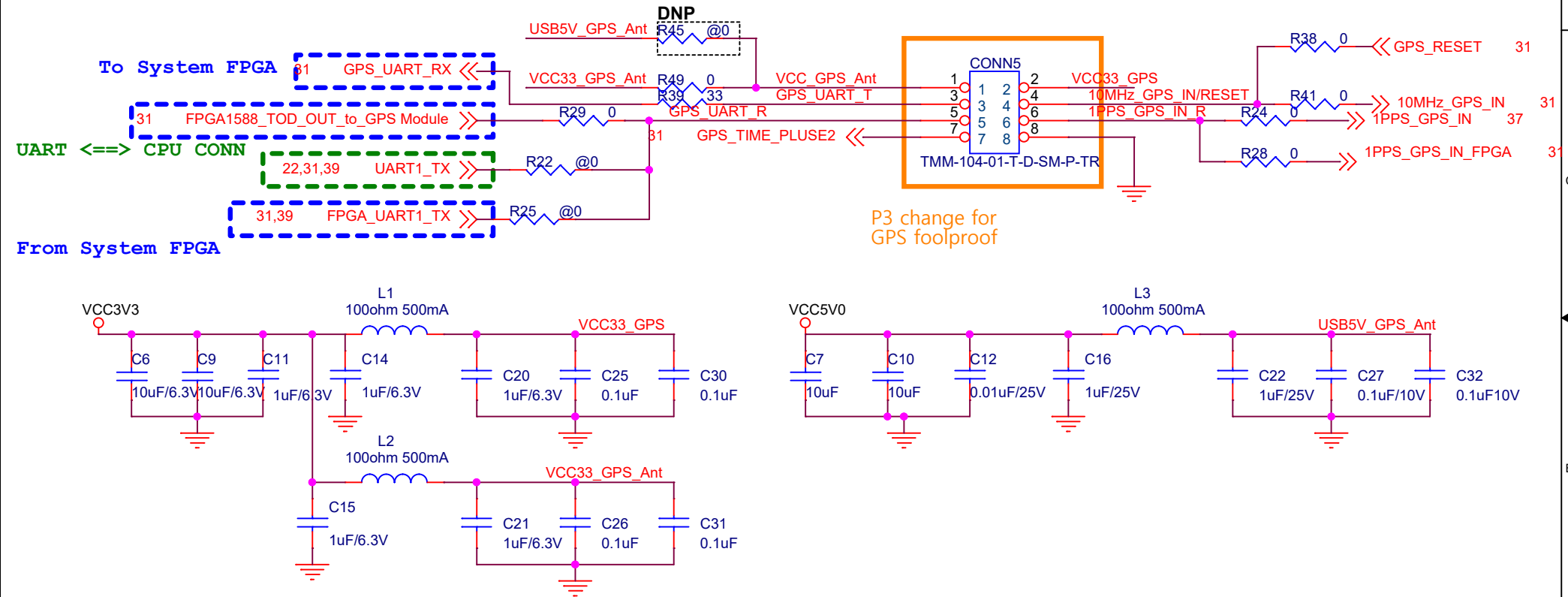


Model Name		AS5915-18X		Rev	R0
Size	C	Page Name	P041_VCC1V0/VCC1V0_ROV_SW		
Date:	Wednesday, January 06, 2021		Sheet	56	of 58



GPS Connector

Note:
1st: 118200000938A TMM-104-01-T-D-SM-P-TR (SAMTEC)
2nd: 118200000937A_DH99-MLB008RL20N-1 (DST)



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Model Name		ES5627BQ-1018-111ZZ	Rev	R0C
Size	Page Name	Engineer		
A	P018_GPS Module	shuanglong_chen		
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